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A REVIEWARTICLE OF SDRAM DESIGN WITH NECESSARY CRITERIA OF DDR CONTROLLER

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ABSTRACT
Double Data Rate Synchronous DRAM (DDR SDRAM) has become a mainstream memory of choice in design due to itsspeed, burst access and pipeline features. The DDR SDRAM is an enhancement to the conventional SDRAM running at bus speed over 75MHz. The DDR SDRAM (referred to as DDR) doubles the bandwidth of the memory by transferring data twice per cycle on both the rising and falling edges of the clock signal. The designed DDR Controller supports data width of 64 bits, Burst Length of 4 and CAS (Column Address Strobe) latency of 2. DDR Controller provides a synchronous command interface to the DDR SDRAM Memory along with several control signals. In this paper, the implementation has been done in Verilog HDL by using Xilinx ISE 9.2i and Modelsim 6.4b.

KEYWORDS: Double Data Rate, Column Address Strobe (CAS), Synchronous Dynamic RAM.

I. INTRODUCTION
A processor is something which processes the given task. It is developed to make human task easy, and when it processes micro things it is called as a microprocessor. It contains basically two things. One is the CPU and second is the memory .CPU stands for central processing unit [1]. It controls the whole processor; we can also call it a human brain. The design of processor needs the designing of CPU and memory. The memory can be static or random. Design of CPU can be done in different ways but its fundamental operation remains the same. CPU is designed on small scale and large scale integration. Processors are designed with enhancements like decreasing power consumption, increasing more pipeline stages, increasing speed and minimizing the chip area. The basic operation performed by a processor is fetching, decoding and executing the given instruction. After that the output will store in memory. For storing the results in memory some mechanism is applied.

With the rapid development in the processor's family, speed and capacity of a memory device is a major concern. The DDR is an enhancement to the traditional synchronous DRAM. The DDR is able to transfer the data on both the edges of each clock cycle. Thus doubling the data transfer rate of the memory device. The DDR is available in a very low cost that's why it is widely used in personal computers where they are basically used to provide the functions of storage and buffers. The DDR SDRAM supports the data widths of 16, 32 and 64 bits. It automatic refresh during the normal and power down modes. The DDR is a complete synchronous implementation of controller. It increases the throughput using command pipelining and bank management. This improvement allows the DDR module to transfer data twice as fast as SDRAM. As an example, instead of a data rate of 133MHz, DDR memory transfers data at 266MHz.DDR modules, like their SDRAM predecessors, arrive in there. Although motherboards designed to implement DDR are similar to those that use SDRAM on motherboards that are designed for DDR. SDRAM, they are not backward compatible with motherboards that support SDRAM. You cannot use DDR in earlier SDRAM based motherboards, nor can you use SDRAM on motherboards that are designed for DDR.

II. MEMORY
Memory unit stores instructions and data. There are mainly two types of memory. The first is volatile and second is non volatile. Random Access Memory (RAM), is a volatile memory that stores information on an

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integrated circuit, whereas ROM (Read only memory) is a non volatile memory and can last longer even after the power is off. The classification of memory is as follows-

A. Random Access Memory

Random access memory (RAM) is the best known form of computer memory. RAM is considered "random access" because you can access any memory cell directly if you know the row and column that intersect at that cell. RAM data, on the other hand, can be accessed in any order. All the data that the PC uses and works with during operation are stored here. Data are stored on drives, typically the hard drives. However, for the CPU to work with those data, they must be read into the working memory storage (RAM).

B. Types of Random Access Memory

Static Random Access Memory

Static Random Access Memory uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory. A flip-flop for a memory cell takes four or six transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes up a lot more space on a chip than a dynamic memory cell. Therefore, you get less memory per chip. Static Random Access Memory uses multiple transistors, typically four to six, for each memory cell but doesn't have a capacitor in each cell. It is used primarily for cache. So static RAM is fast and expensive, and dynamic RAM is less expensive and slower. So, static RAM is used to create the CPU's speed-sensitive cache, while dynamic RAM forms the larger system RAM space.

Dynamic Random Access Memory

Dynamic Random Access Memory has memory cells with a paired transistor and capacitor requiring constant refreshing. DRAM works by sending a charge through the appropriate column (CAS) to activate the transistor at each bit in the column. When writing the row lines contain the state the capacitor should take on. When reading the sense amplifier determines the level of charge in the capacitor. If it is more than 50 percent, it reads it as a 1 otherwise it reads it as a 0.

A memory chip rating of 70ns means that it takes 70 nanoseconds to completely read and recharge each cell. It is one of the most common types of computer memory (RAM). It can only hold data for a short period of time and must be refreshed periodically. DRAMs are measured by storage capability and access time. Storage is rated in megabytes (8 MB, 16 MB, etc). Access time is rated in nanoseconds (60ns, 70ns, 80ns, etc) and represents the amount of time to save or return information. With a 60ns DRAM, it would require 60 billionths of a second to save or return information. The lower the speed, the faster the memory operates. DRAM chips require two CPU wait states for each execution. Can only execute either a read or write operation at one time. The capacitor in a dynamic RAM memory cell is like a leaky bucket. It needs to be refreshed periodically or it will discharge to 0. This refresh operation is where dynamic RAM gets its name. Memory is made up of bits arranged in a two-dimensional grid. In which memory cells are fetched onto a silicon wafer in an array of columns (bit lines) and rows (word lines).

The intersection of a bit line and word line constitutes the address of the memory cell. Memory cells alone would be worthless without some way to get information in and out of them. So the memory cells have a whole support infrastructure of other specialized circuits. Identifying each row and column (row address select and column address select) Keeping track of the refresh sequence (counter) Reading and restoring the signal from a cell (sense amplifier) Telling a cell whether it should take a charge or not (write enable) Other functions of the memory controller include a series of tasks that include identifying the type, speed and amount of memory an checking for errors. The traditional RAM type is DRAM (dynamic RAM). The other type is SRAM (static RAM). SRAM continues to remember its content, while DRAM must be refreshed every few milliseconds.

Double Data Rate Synchronous Dynamic Random Access Memory

Double Data Rate Synchronous Dynamic Random Access Memory is the original form of DDR SDRAM. It is just like SDRAM except that is has higher bandwidth, meaning greater speed. Maximum transfer rate to L2 cache is approximately 1,064 MBps (for DDR SDRAM 133 MHZ). DDR RAM is clock doubled version of SDRAM, which is replacing SDRAM during 2001- 2002. It allows transactions on both the rising and falling edges of the clock cycle. It has a bus clock speed of 100MHz and will yield an effective data transfer rate of 200MHz. DDR come in PC 1600, PC 2100, PC 2700 and PC 3200 DIMMs. A PC 1600 DIMM is made up of

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PC 200 DDR chips, while a PC 2100 DIMM is made up of PC 266 chips. Go for PC2700 DDR. It is about the cost of PC2100 memory and will give you better performance.

DDR memory comes in CAS 2 and CAS 2.5 ratings, with CAS costing more and performing better. This paper is organized as follows. Block diagram of DDR controller will be described. The architecture of DDR controller will be described in, different functional blocks will be explained. Finally the Result and Conclusion will be given in and respectively.

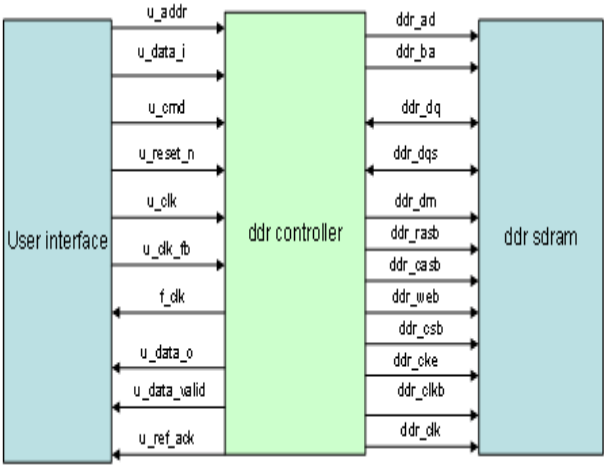

Fig 1.2 Top Level block diagram

Control unit

All operations of processors are controlled by this unit. It actually generates timing signals which determines when the operation is going to take place. The interfacing of components with external elements is also done by this unit. It can be hardwired or micro programmed. But hardwired controllers are fast. The functions of control unit are as follows-

- Control unit has communication among all components of the processor.
- It instructs the arithmetic logic unit that which type of operation is to be performed.
- It coordinates with peripherals of the processor.
- It directs all components to perform action.
- It regulates the flow of data between main memory and other units.

III. DESIGN RULES IN VLSI

The rules are made to check whether the design is correct or not. After full verification of each rule the design goes to the fabrication lab for fabrication. This process is called as Electronic design Automation. These rules basically check layout not the schematic [12]. There are lambda based rules, Meta rules and micro based rules. Amongst them most popular is lambda based rules. These rules play an important role because they are an interface between design engineers and fabrication engineers. There are design rules checking software. There are basic three rules for width, length and masks. Some of the lambda rules are as follows-

- Well to well spacing should be 2 χ
- Well to poly spacing should be 2 χ
- Well to metal spacing should be 3 χ
- Poly-active minimum spacing should be 1 χ
- Poly overlap spacing should be 2 χ

IV. PIPELINING PROCESSORS

The pipelining is a kind of parallel processing used to increase the speed of the processor. It can be either software or hardware. It consists of some stages one after another [4]. With pipeling much of the time is saved from processing, improves speed of processor a lot. We can divide the pipe into several segments, where each of the segments is dependent on the other. We can add more no of segments as per need but taking care of pipeline hazards.

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V. ISSUE OF OLD ARTICLES

The most important thing is not only there structure but the timing relations of input and output, there are some requirements with hardware description language then only we can appreciate the language. The four requirements are abstraction, modularity, concurrency and hierarchy [5].

VHDL is used to write text models that describe a logic circuit. There is a simulation program for test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly called a test bench. VHDL has filed input and output capabilities, and can be used as a general-purpose language for text processing, but files are more commonly used by a simulation test bench for stimulus or verification data. In this case, it might be possible to use VHDL to write a test bench to verify the functionality of the design using files on the host computer to define stimuli, to interact with the user, and to compare results with those expected. Many designers leave this job to the simulator. VHDL is a Dataflow language which all runs sequentially, one instruction at a time. It is capable of describing very complex behavior. For designing any digital system VHDL is the best language. Pipeling is something we come across day to day life. To design a CPU we need instruction set, no of registers and their details, datapath i.e. data will from which source to which destination and the control circuits for execution of instructions there can be two types hardware control signals and software control signals. Distributed computer is mostly used. We want to do more no of tasks in less amount of time for that we require a new concept i.e. pipelining which will help in reducing execution time.

The most important thing is not only there structure but the timing relations of input and output [3]. There are some requirements with hardware description language then only we can appreciate the language. The four requirements are abstraction, modularity, concurrency and hierarchy. VHDL is used to write text models that describe a logic circuit. There is a simulation program for test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly design and verification of digital circuits at higher register-transfer level of abstraction. It is also used in the verification of analog circuit and mixed-signal circuits, as well as in the design of genetic circuits [7].

In the design implementation of 16 bit CPU the clock period is highly reduced as called a test bench. VHDL has filed input and output capabilities, and can be used as a general-purpose language for text processing, but files are more commonly used by a simulation test bench for stimulus or verification data. In this case, it might be possible to use VHDL to write a test bench to verify the functionality of the design using files on the host computer to define stimuli, to interact with the user, and to compare results with those expected. Many designers leave this job to the simulator. VHDL is a Dataflow language which all runs sequentially, one instruction at a time. It is capable of describing very complex behavior. For designing any digital system VHDL is the best language [5].

VI. MACHINE STATE DIAGRAM

Initially the controller is in the IDLE state. That means no operation is performing. A PRECHARGE ALL command is then applied. This command is used to deactivate any open row in a bank or the open bank row in all banks. Once a bank is pre charged, it is in idle state and must be activated prior to any READ and WRITE operation. Next a LOAD MODE REGISTER command should be issued for the extended mode register to enable the DLL, then another LOAD MODE REGISTER command to the mode register to reset the DLL and to program the operating parameters. Again a PRECHARGE command should be applied which place the device in all banks in IDLE state. In the IDLE state two AUTO REFRESH cycles must be performed.

VII. CONCLUSION

In this paper an efficient fully functional DDR SDRAM controller is designed. The controller generates different types of timing and control signals, which synchronizes the timing and control the flow of operation. The memory system operates at double the frequency of processor, without affecting the performance. Thus we can reduce the data bus size. The drawback of this controller is complex schematic with large number of buffers in the circuit increases the amount of delay

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